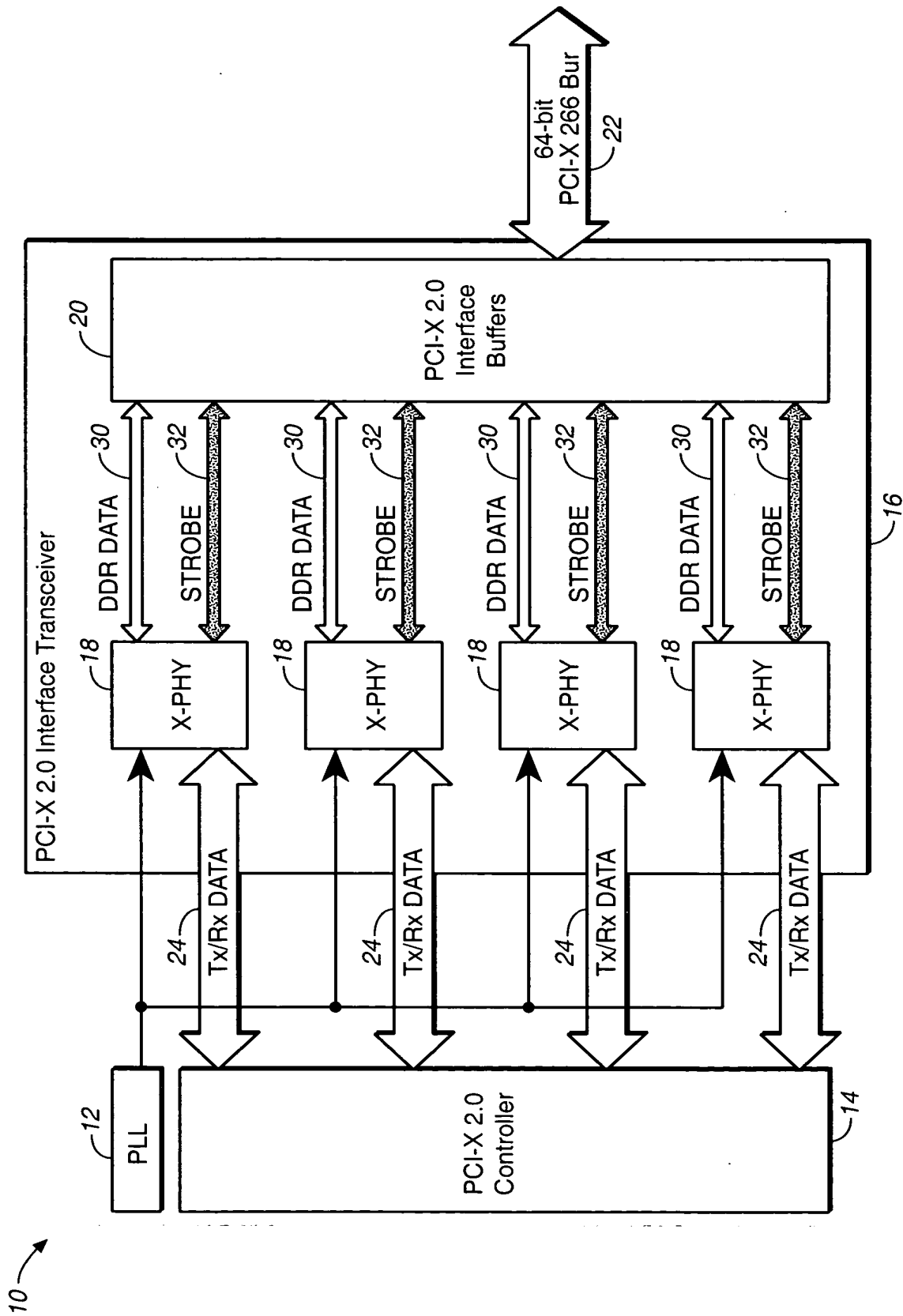


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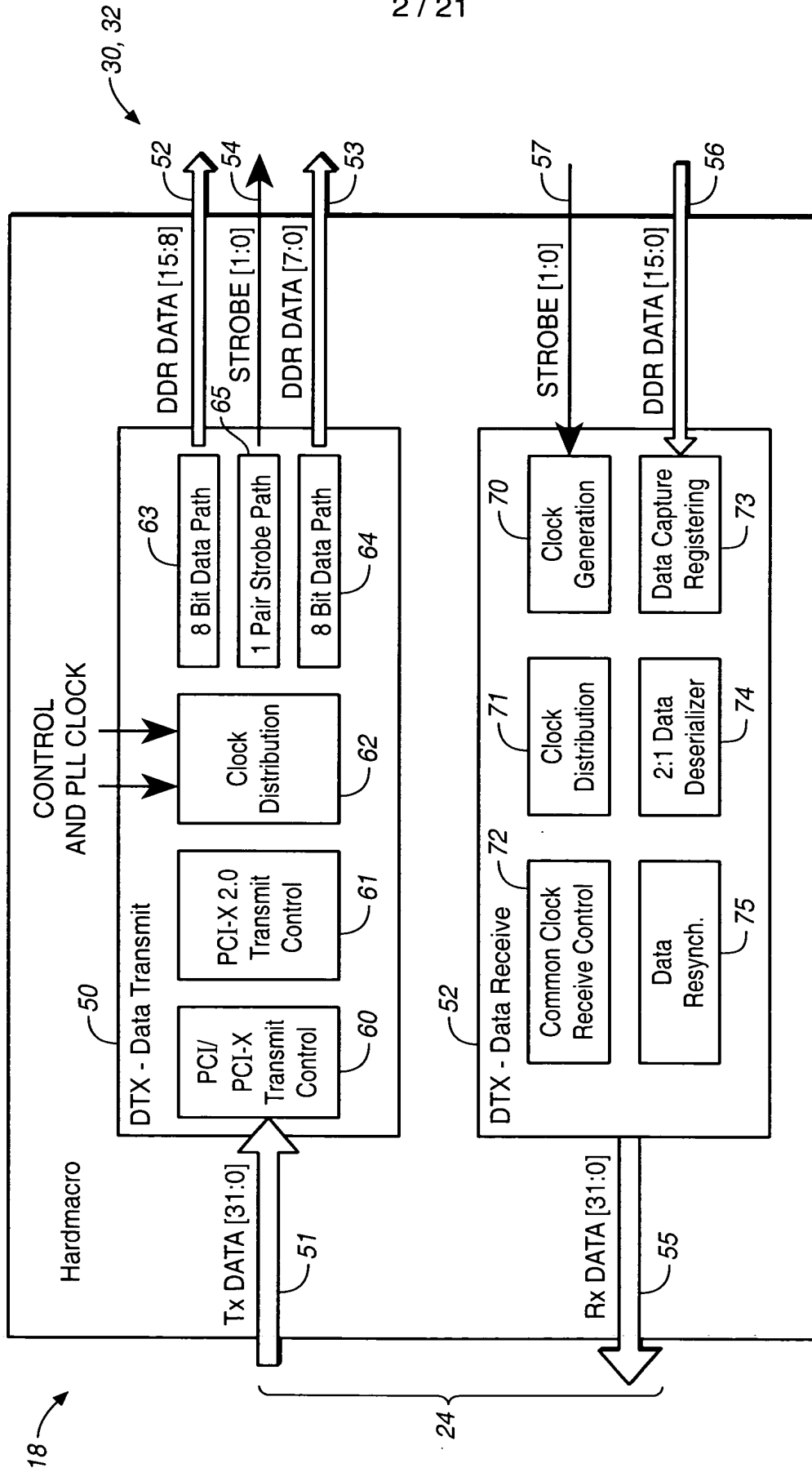
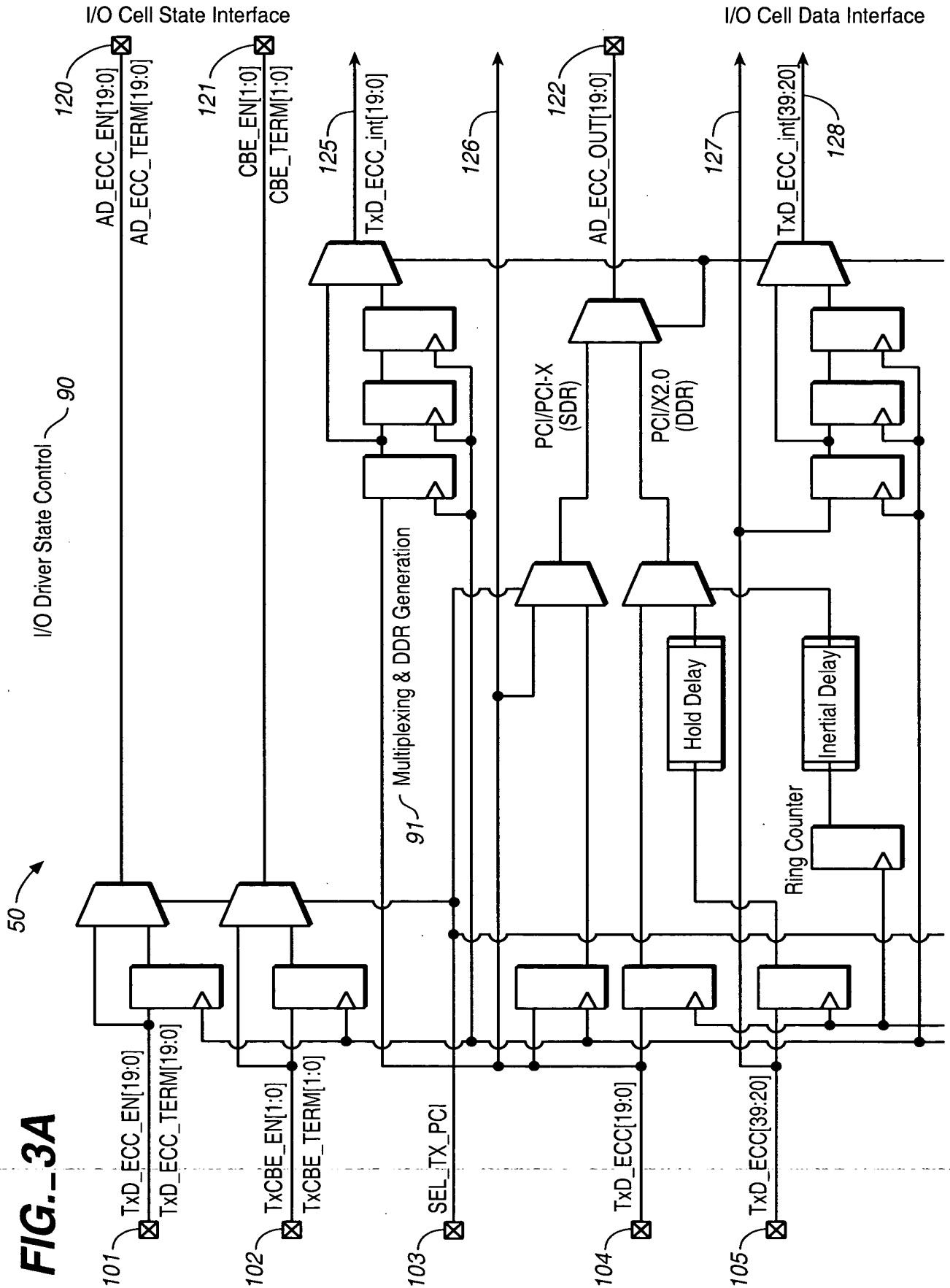


FIG..2

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FIG. 3A



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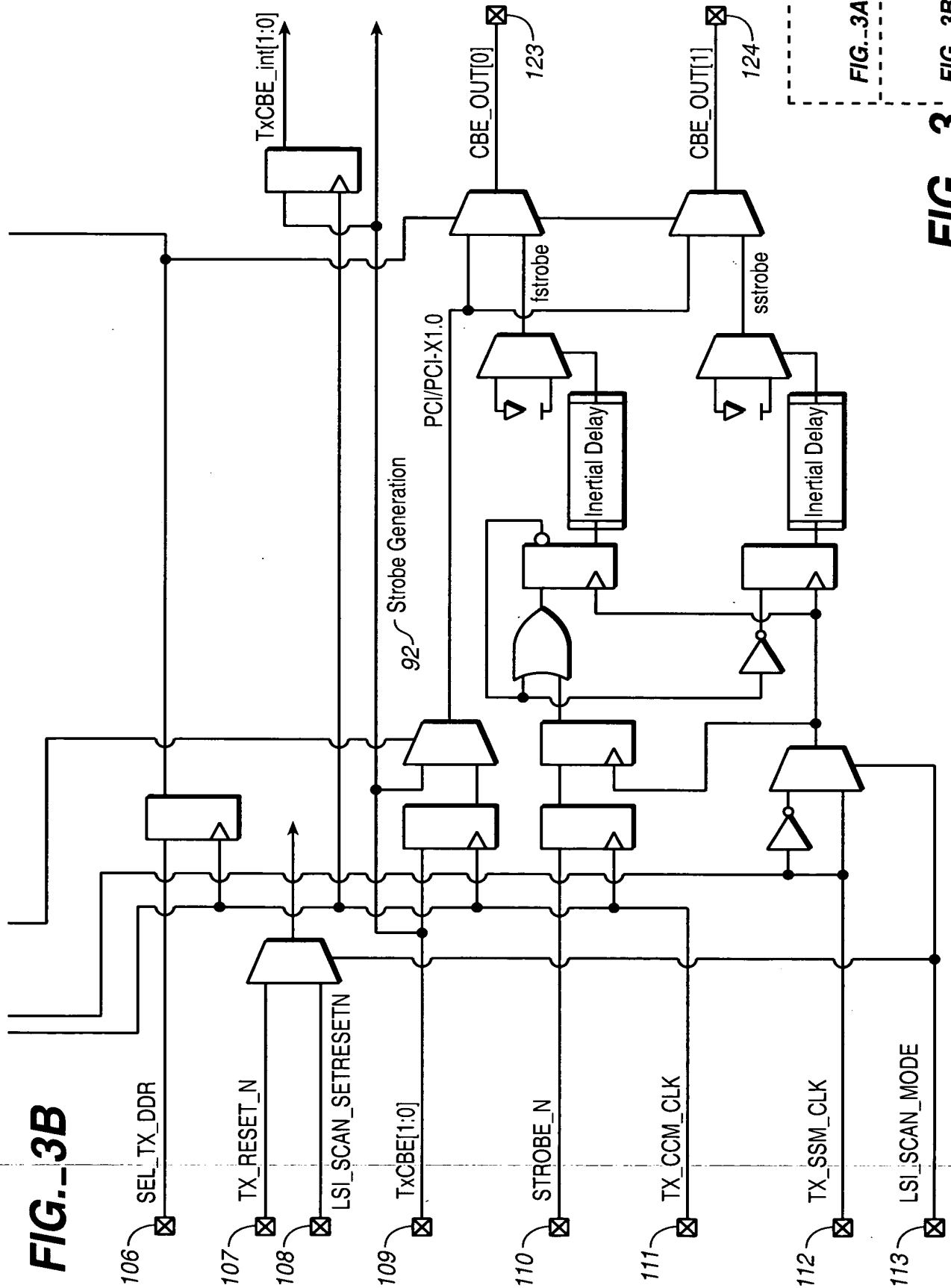
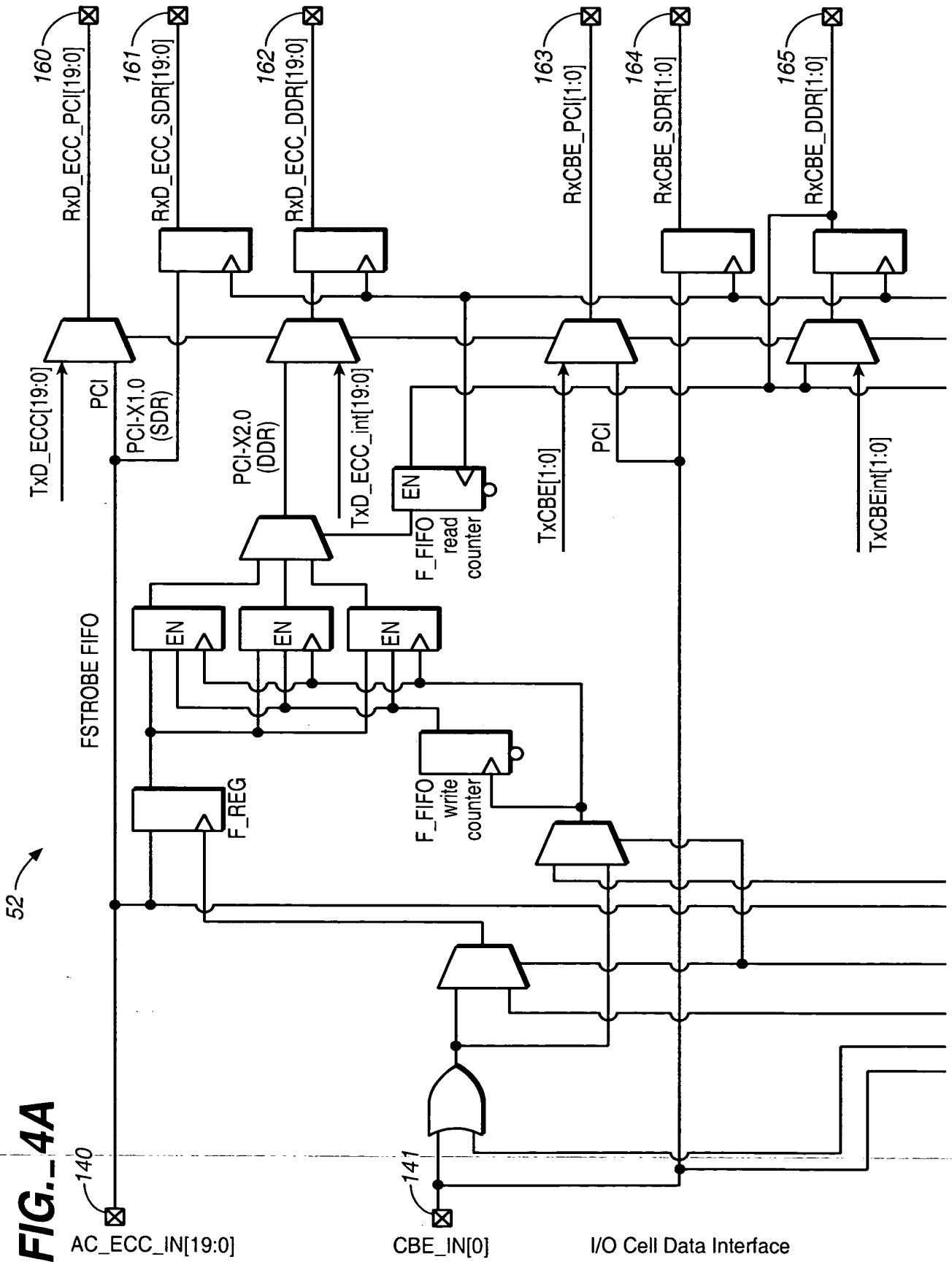


FIG._3

FIG._3A

FIG._3B

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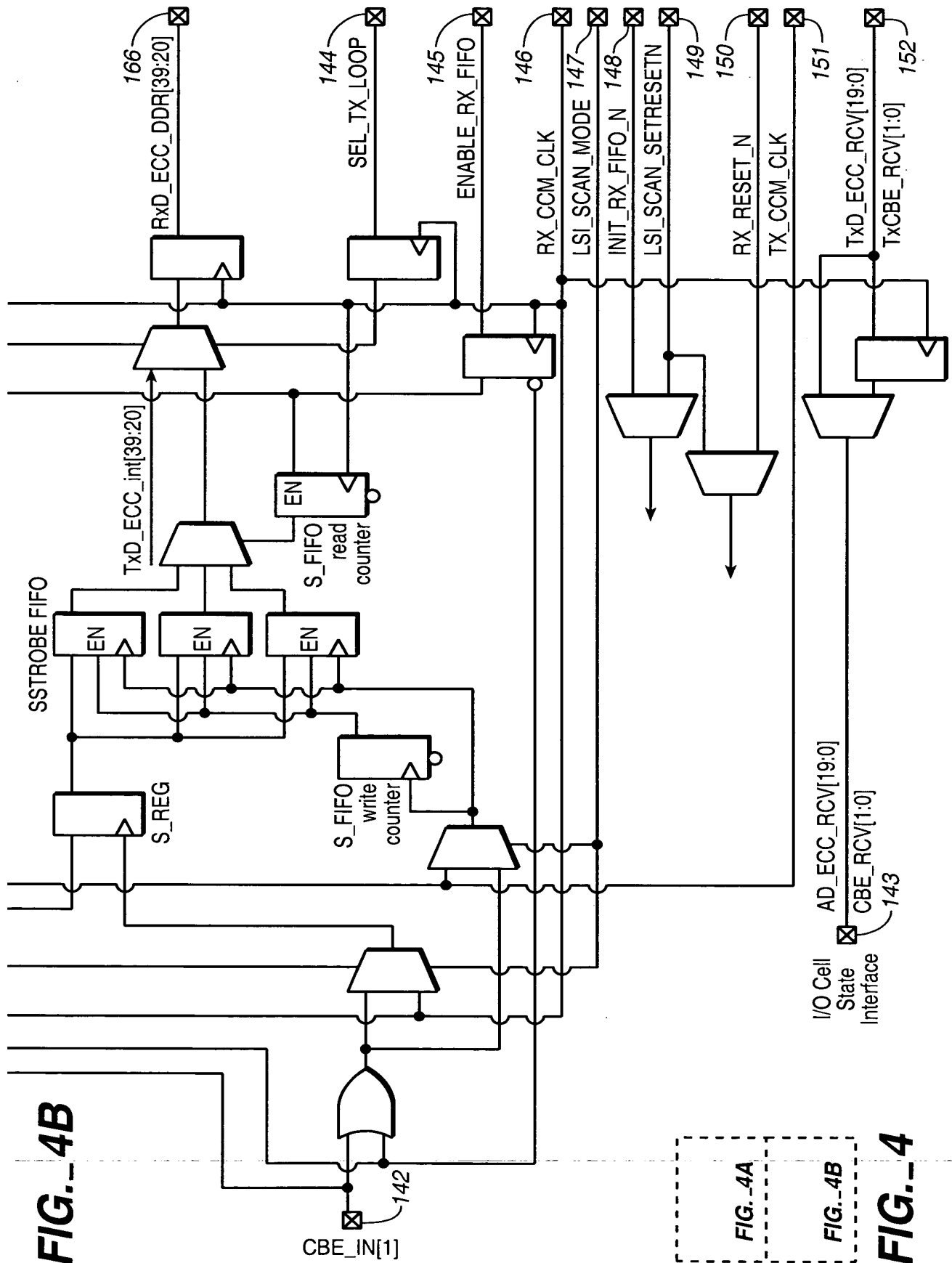


FIG._5

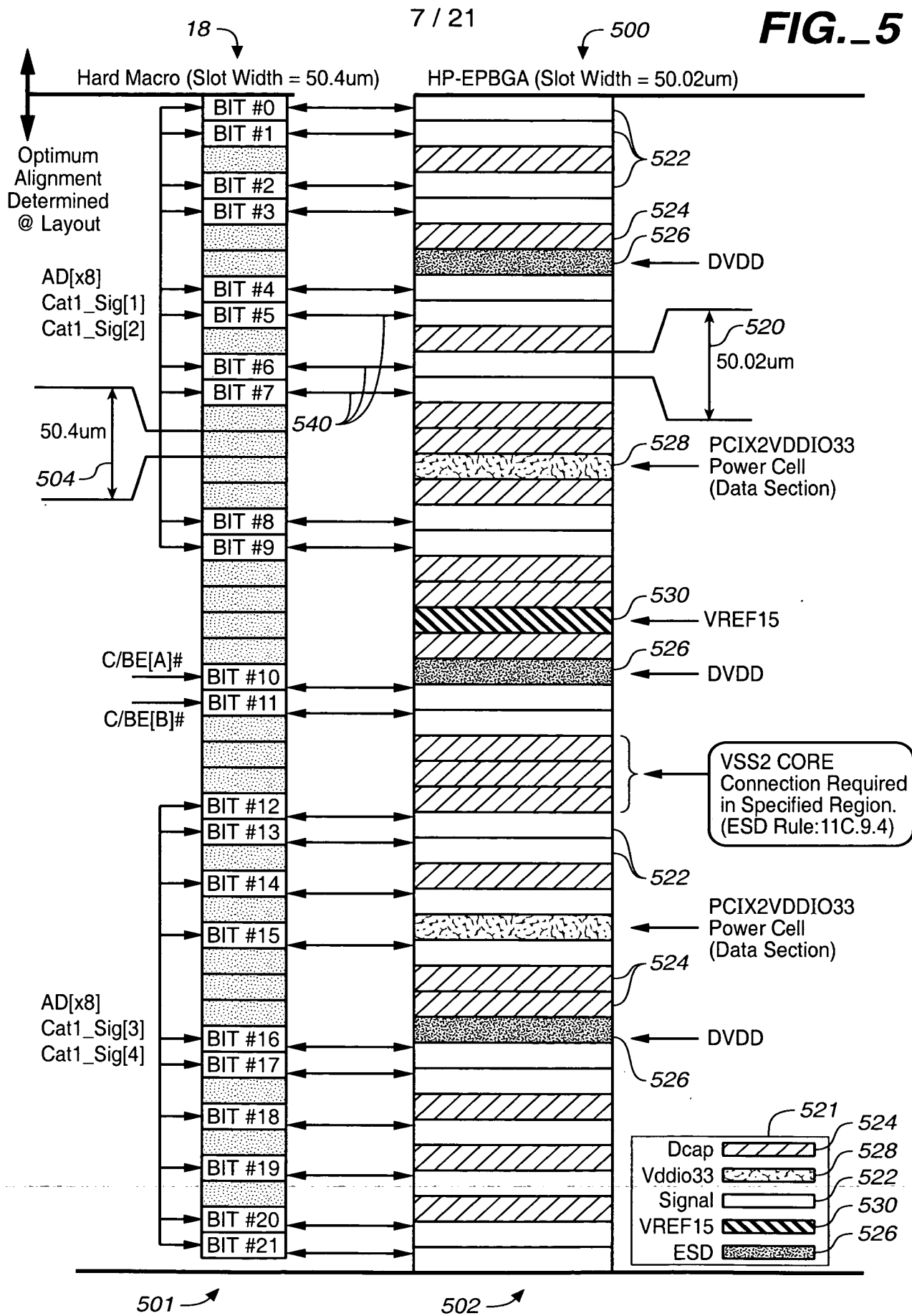


FIG._6

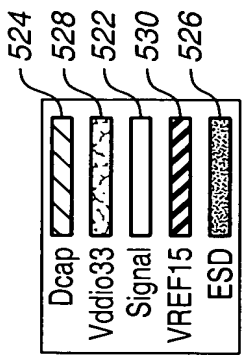
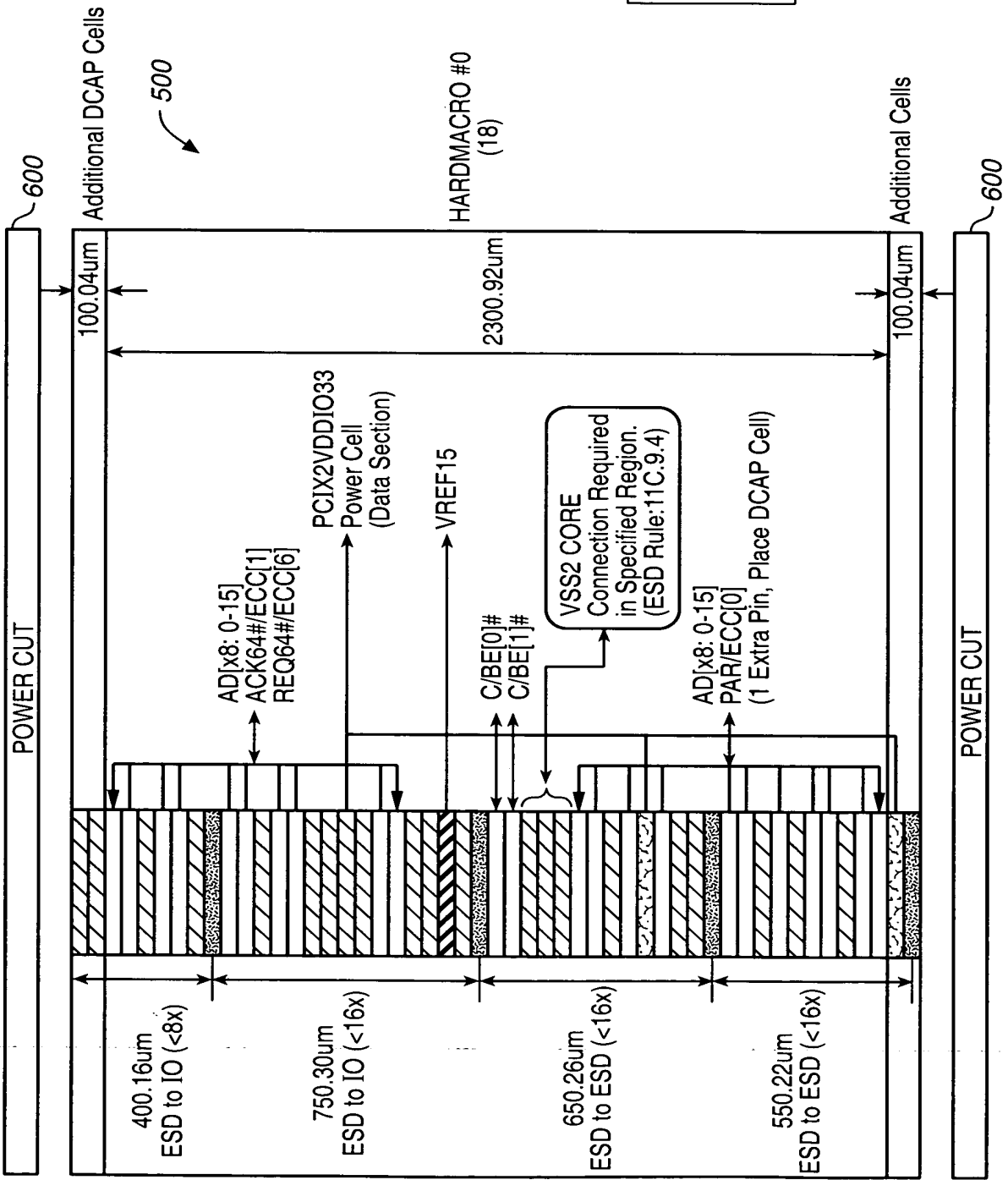
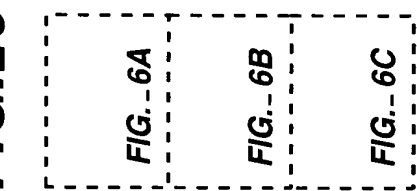


FIG._6A

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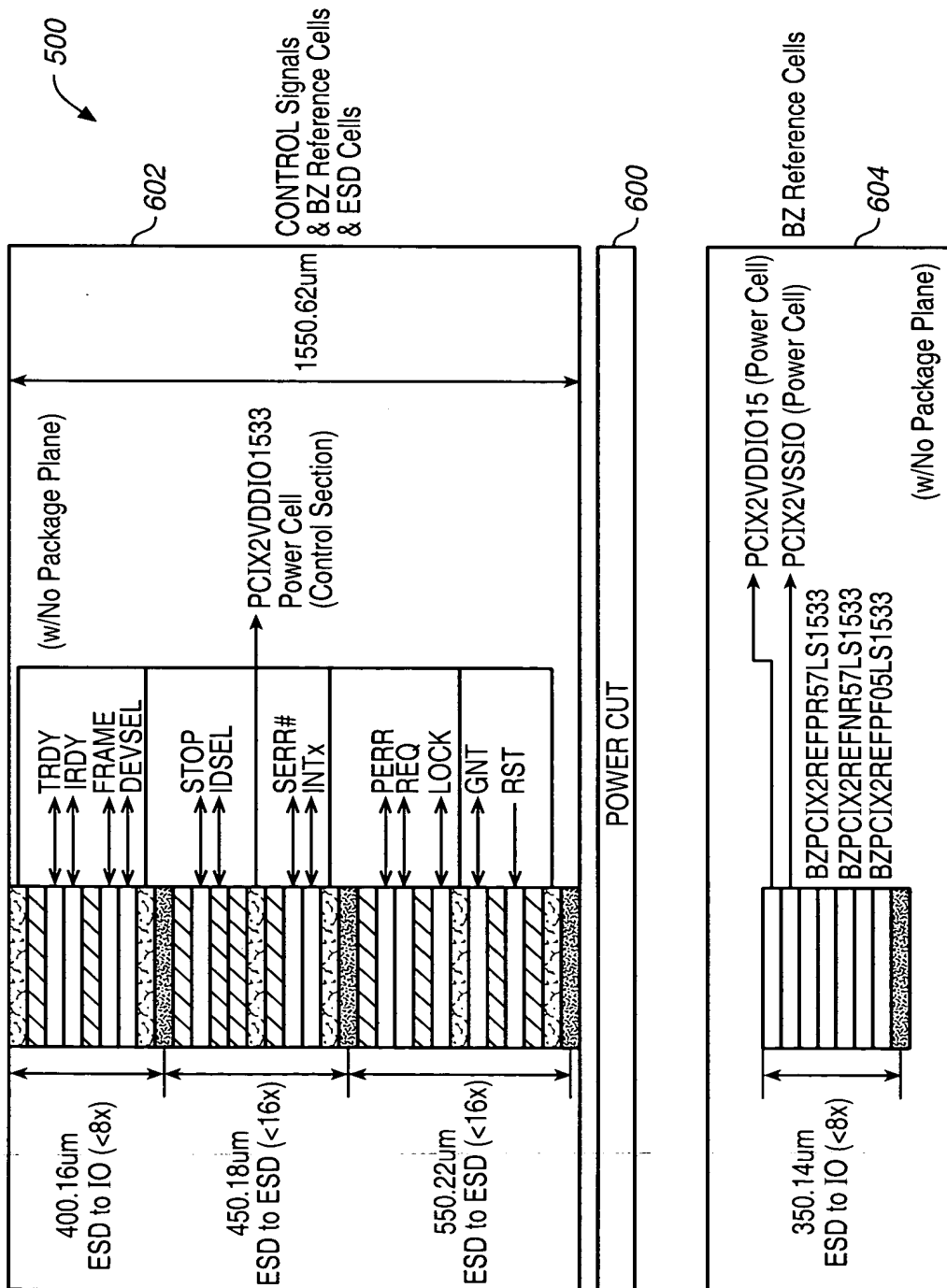


FIG. 6B

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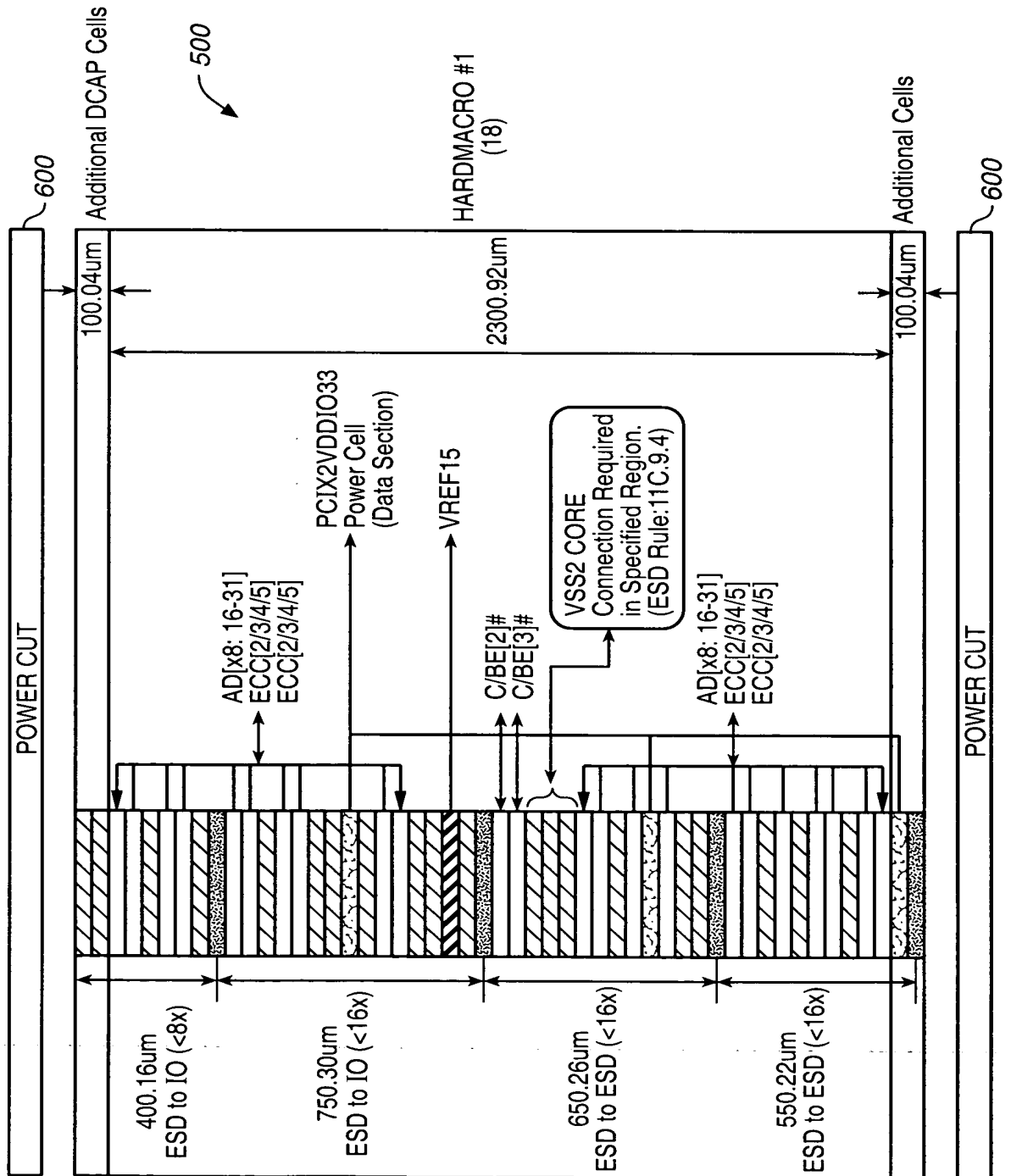
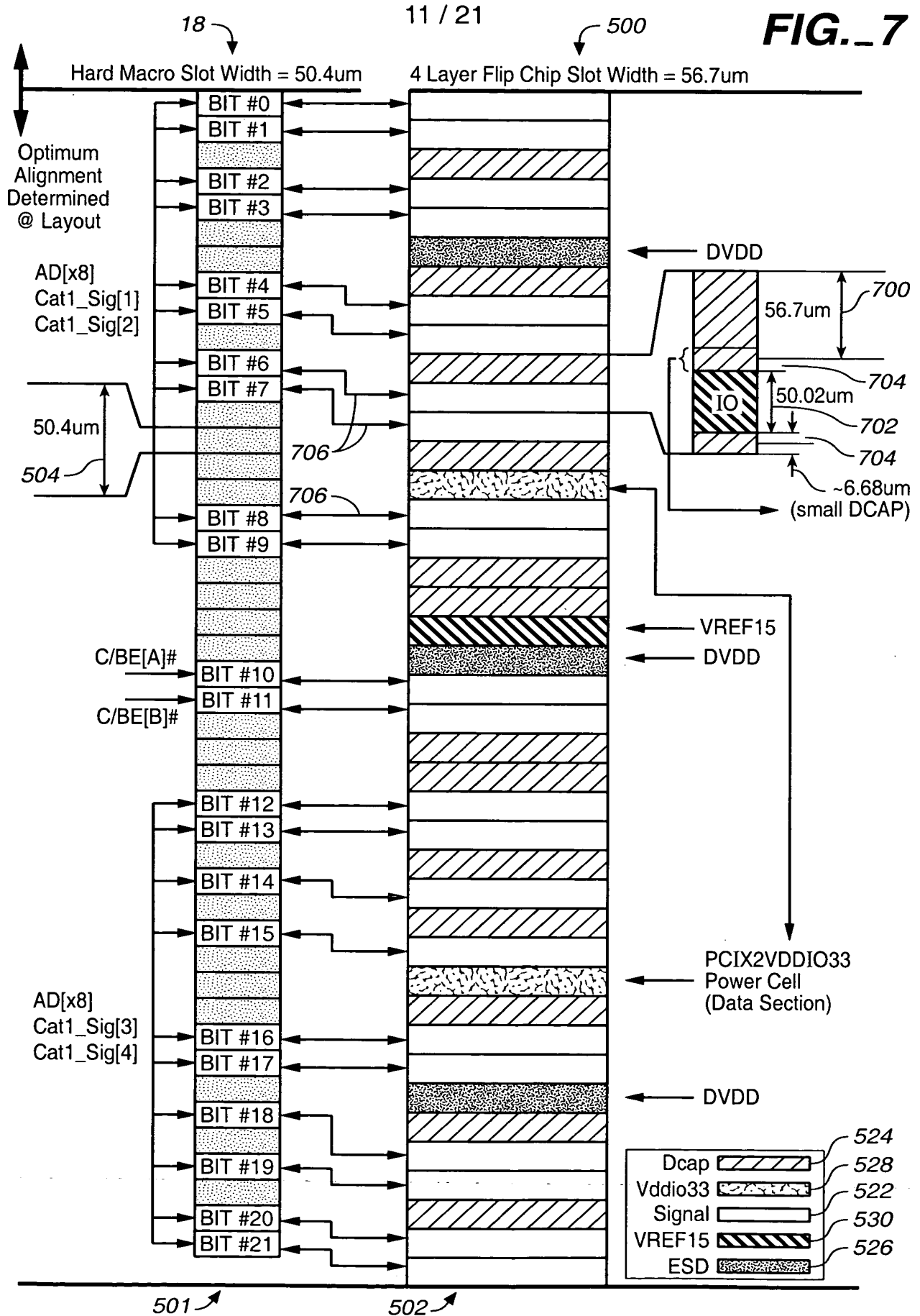


FIG. 6C



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FIG. 8

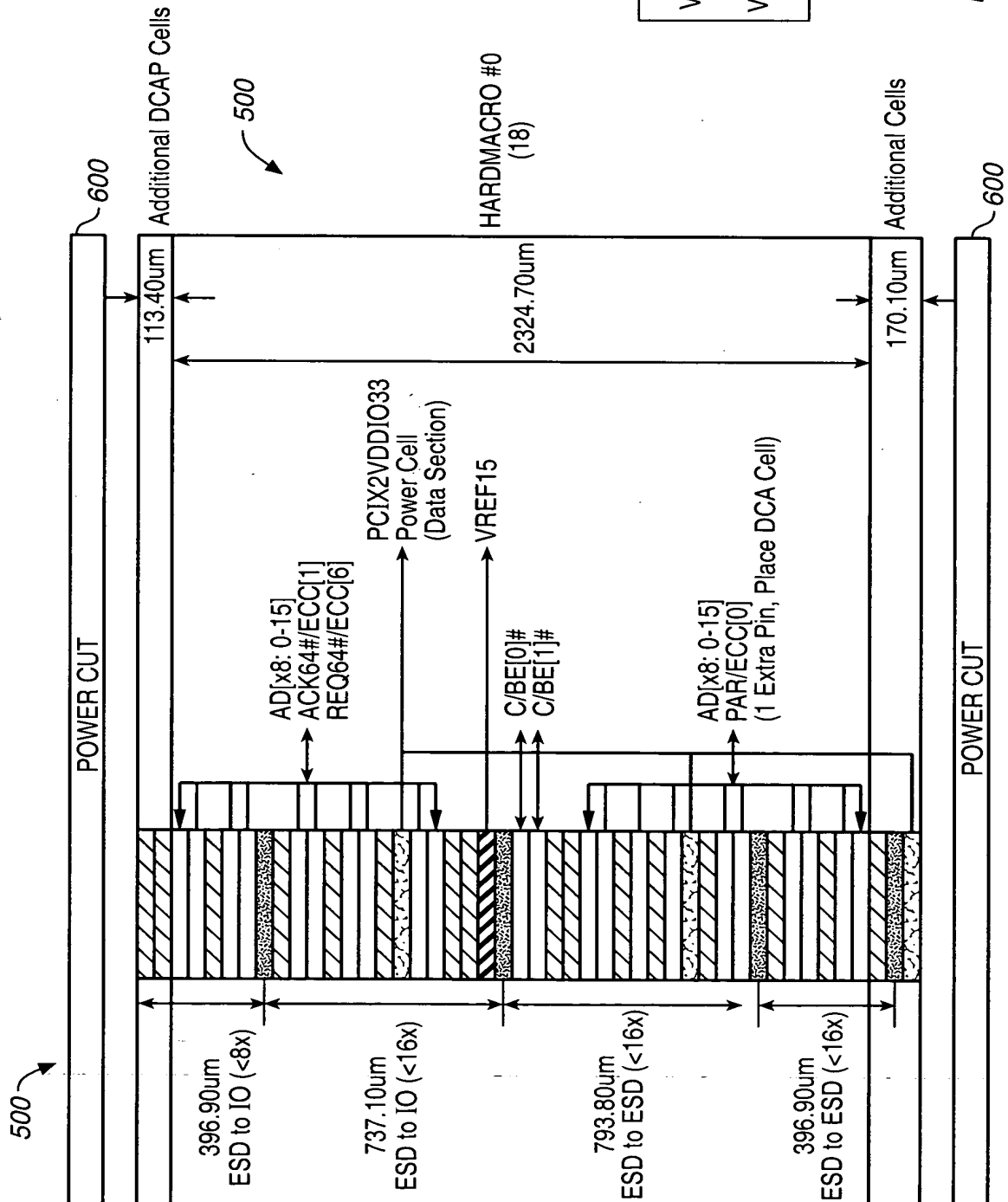
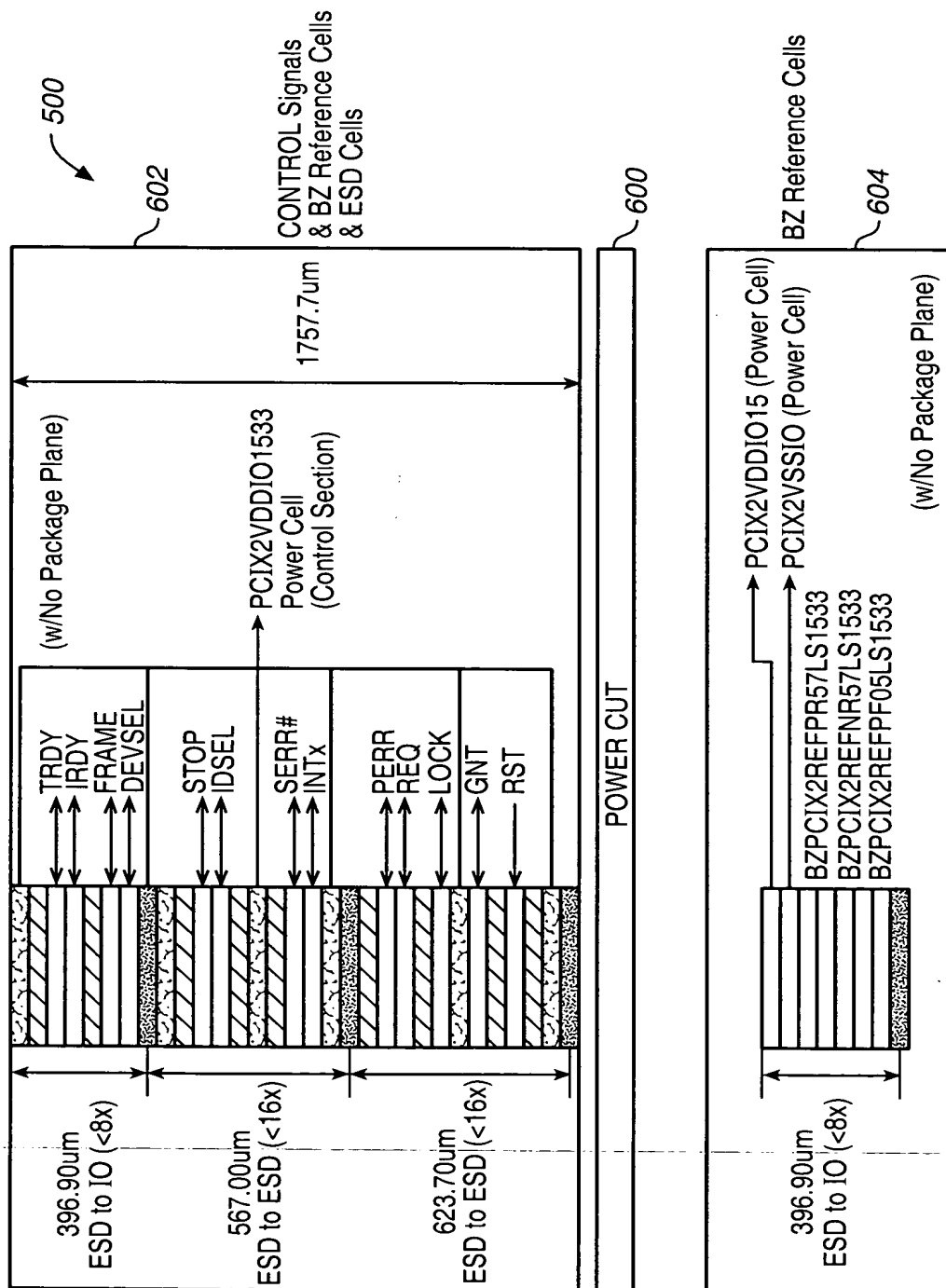


FIG. 8A

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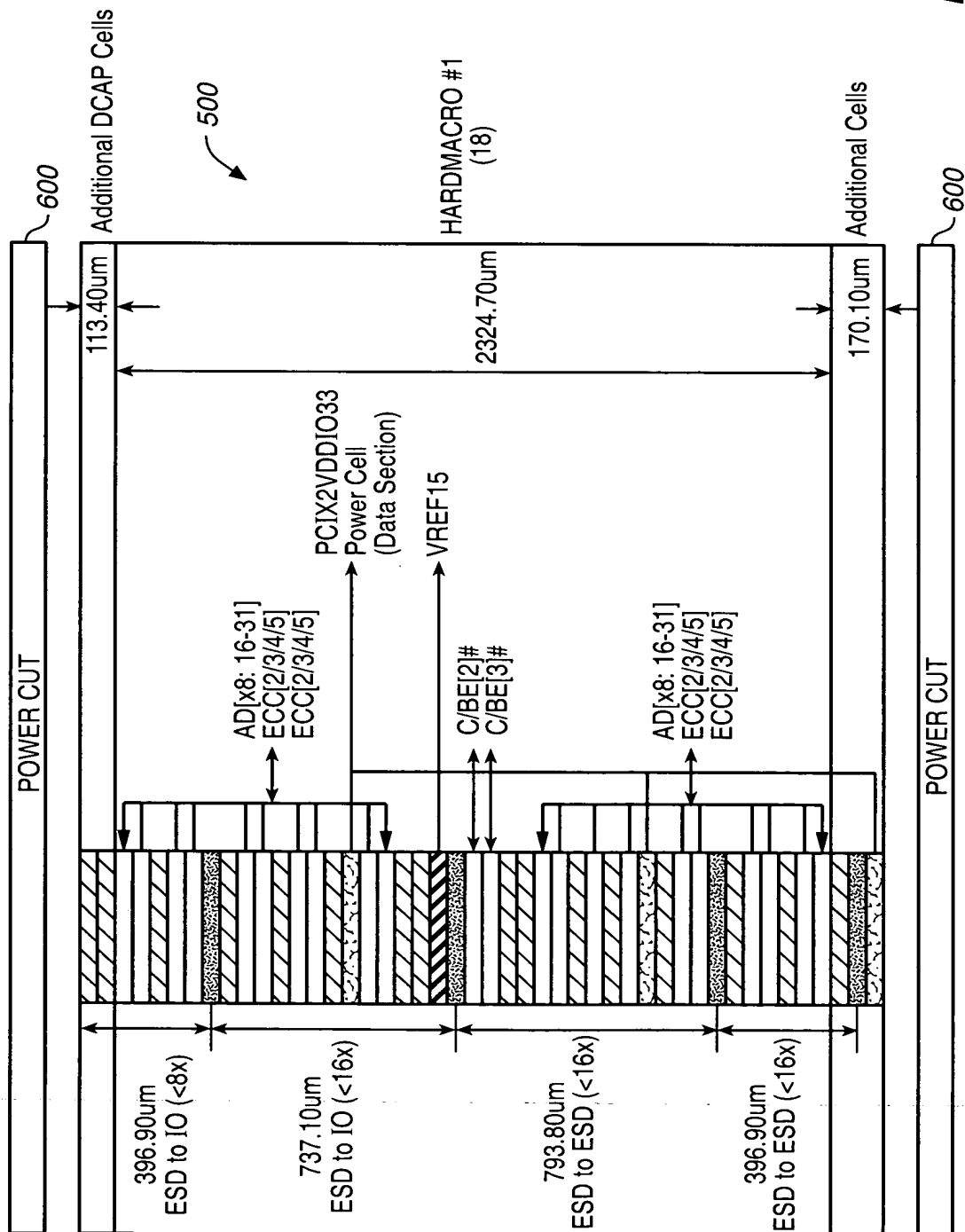


FIG. 8C

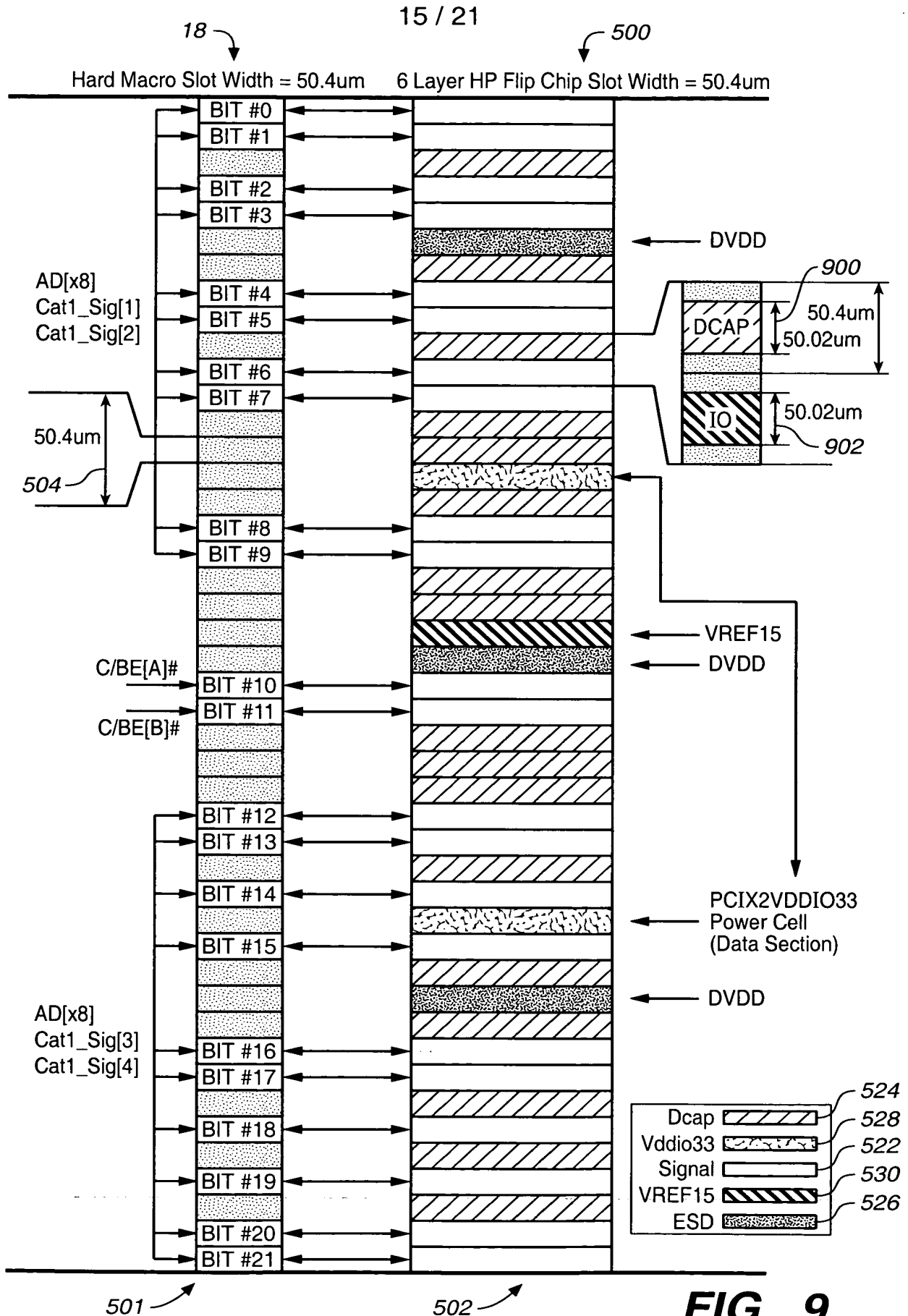


FIG._9

FIG. 10

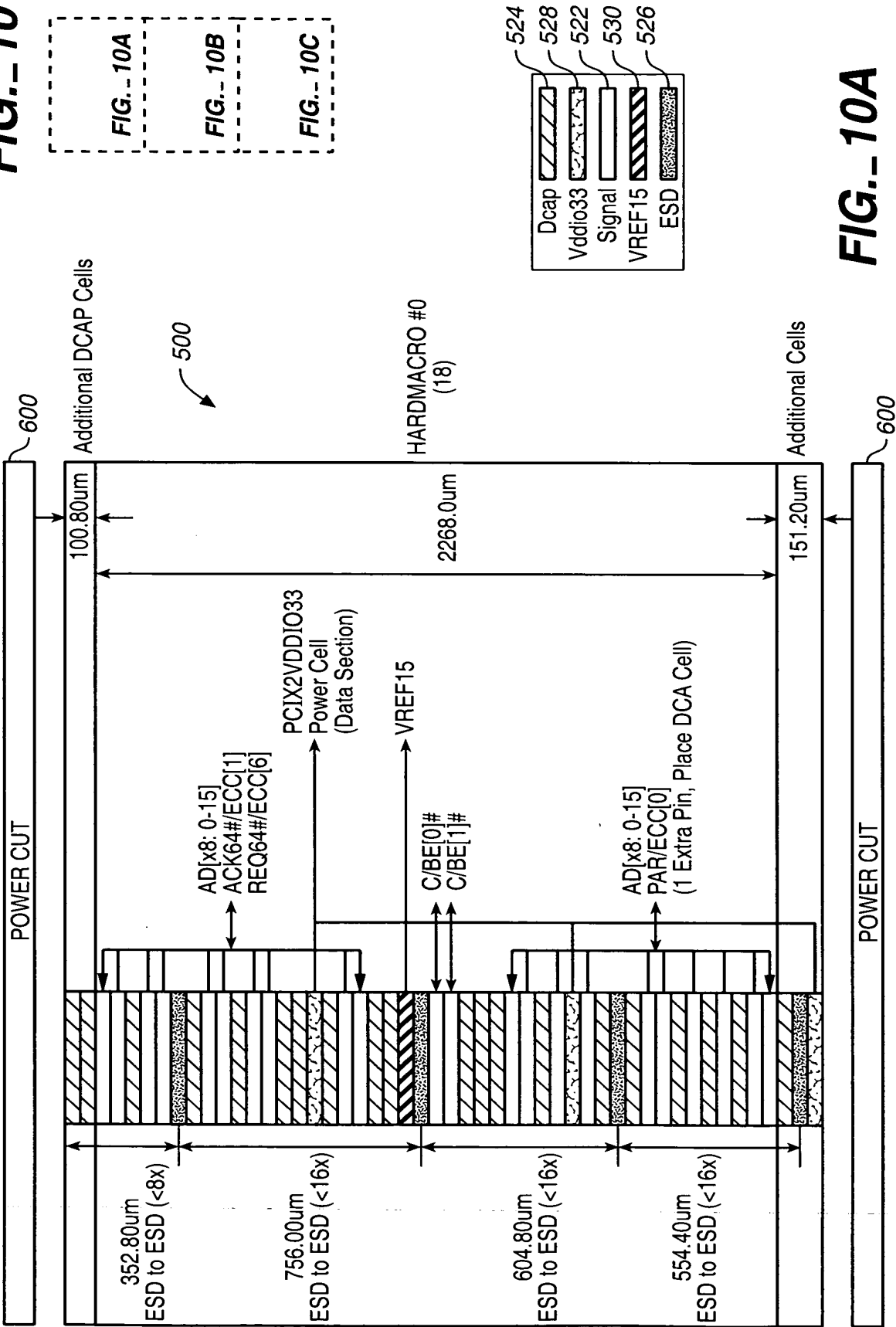


FIG. 10A

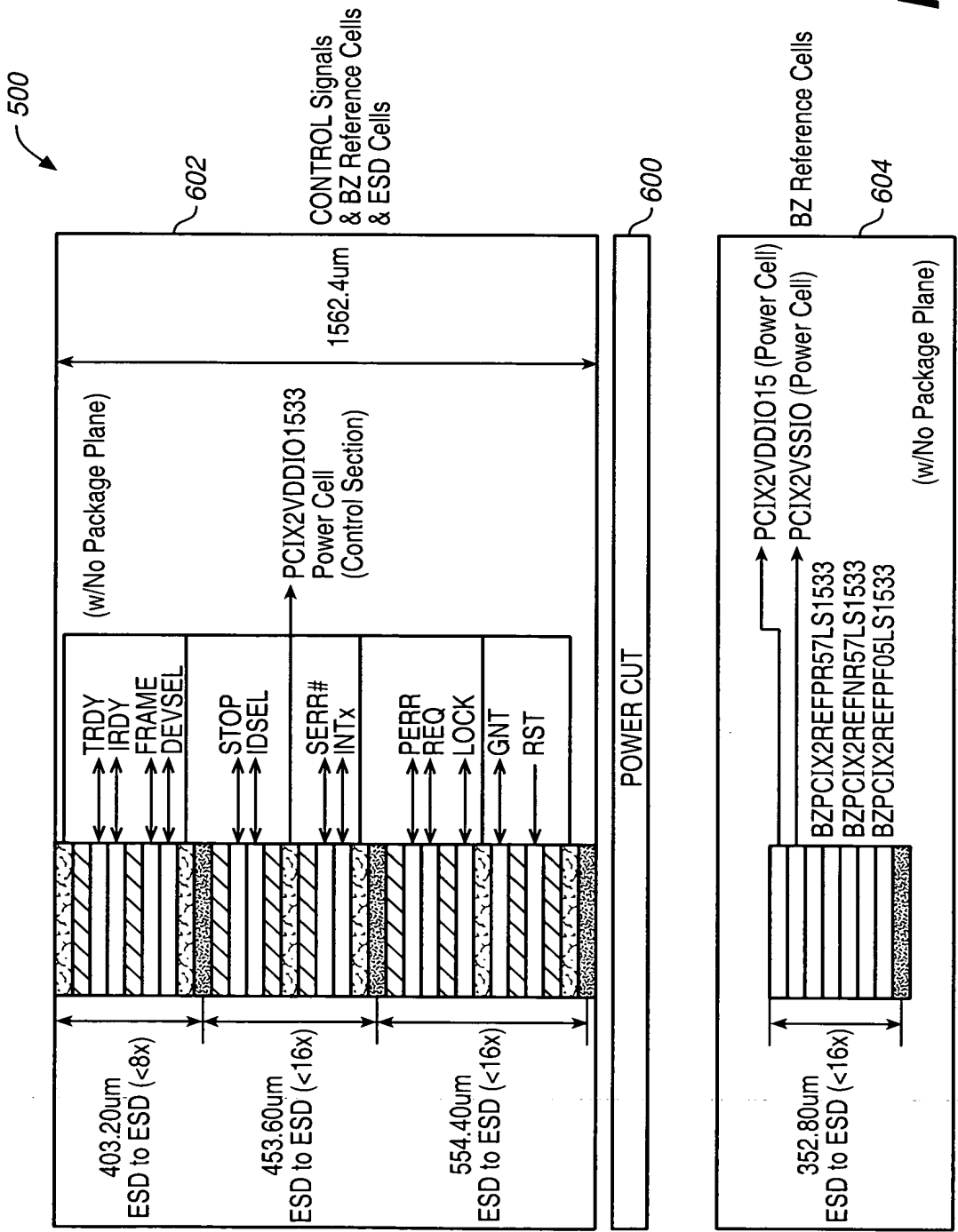


FIG.- 10B

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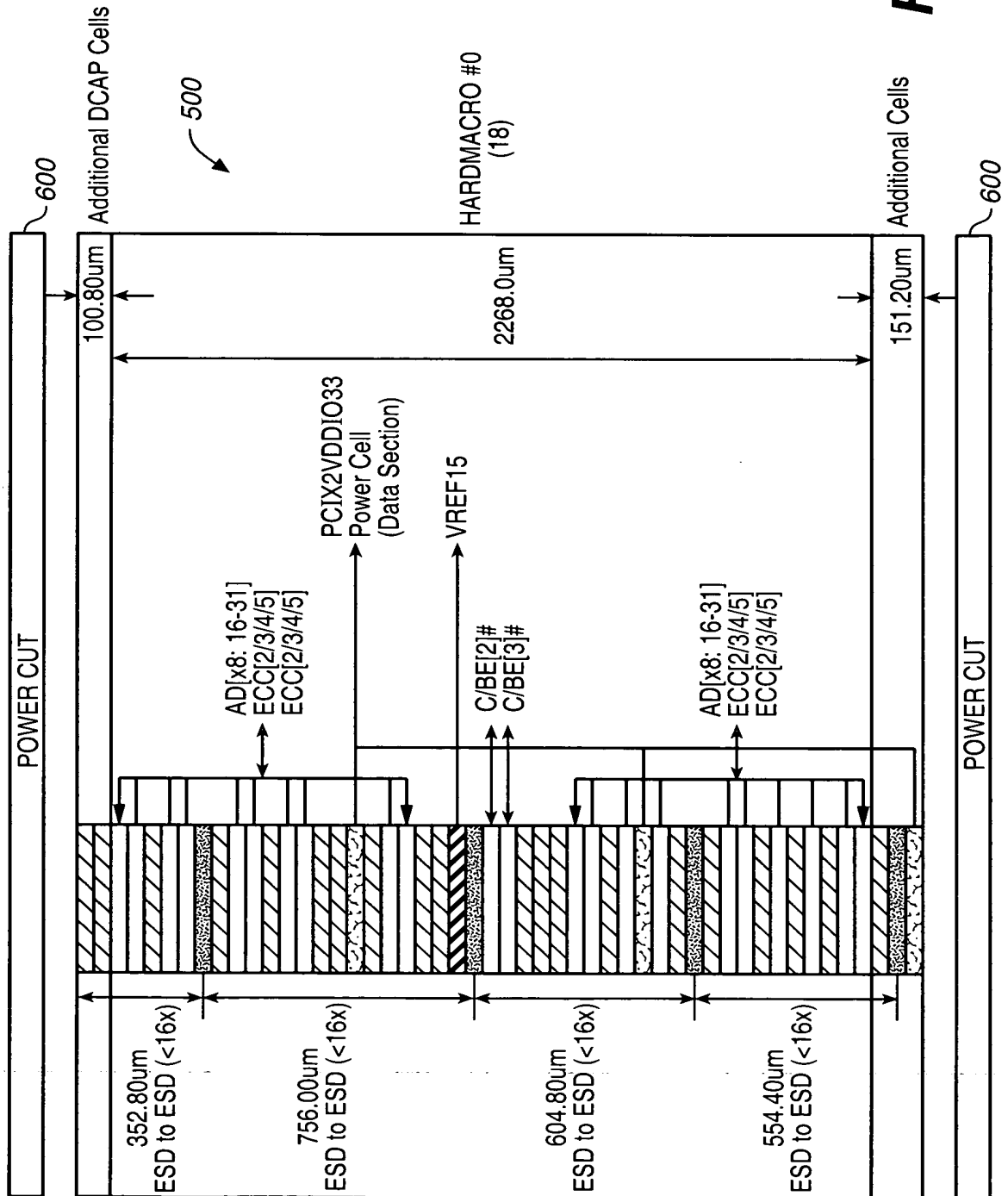
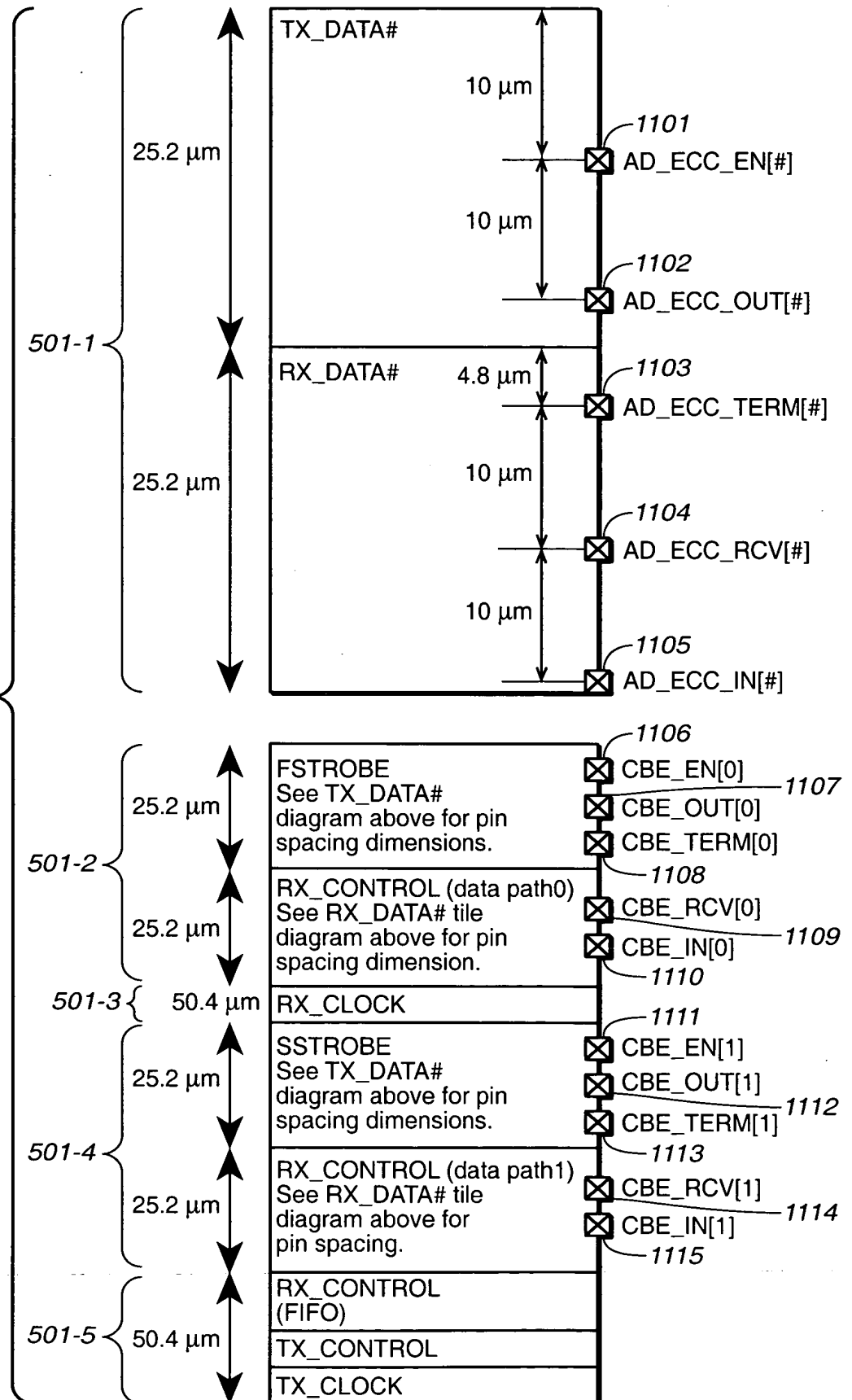


FIG. 10C

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Data Path Instance Pin Locations

FIG._11



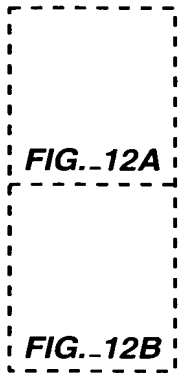


FIG._12

FIG._12A

Top Level Floor Plan

LSI_SCAN_IN[2:0]

Data path instance pins:

TxD_ECC_EN[#]
TxD_ECC_TERM[#]
TxD_ECC_RCV[#]

RxD_ECC_PCI[#]
TxD_ECC[#]
RxD_ECC_DDR[#]
RxD_ECC_SDR[#]
TxD_ECC[#]
RxD_ECC_DDR[#]

Scan input routing
TX_DATA0
RX_DATA0

AD_ECC_EN[0]
AD_ECC_OUT[0]
AD_ECC_TERM[0]
AD_ECC_RCV[0]
AD_ECC_IN[0]

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Control and clock
instance pins:

TxCBE_EN[#]
TxCBE_TERM[#]
TxCBE_RCV[#]

RxCBE_PCI[#]
TxCBE[#]
RxCBE_DDR[#]
RxCBE_SDR[#]

STROBE_N
SEL_TX_LOOP
ENABLE_RX_FIFO
SEL_TX_DDR
SEL_TX_PCI

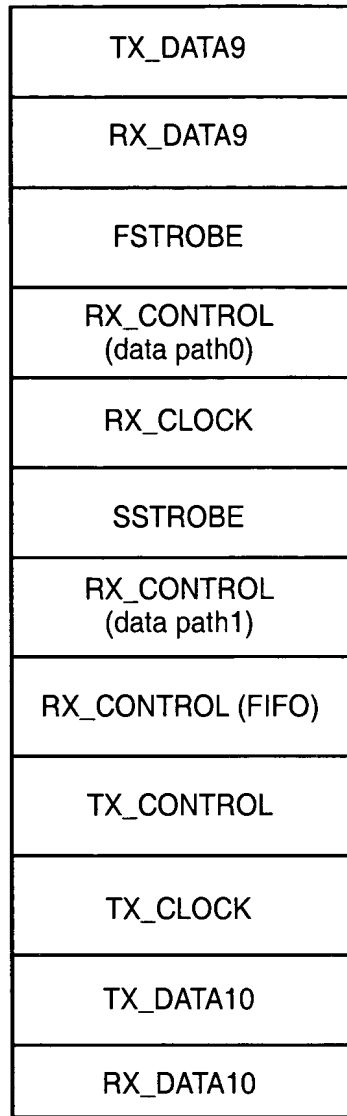
LSI_SCAN_MODE
LSI_SCAN_SETRESETIN
TX_RESET_N
TX_CCM_CLK
TX_SSM_CLK
LSI_SCAN_ENABLE
RX_RESET_N
INIT_RX_FIFO_N
RX_CCM_CLK

Data path instance pins:

TxD_ECC_EN[#]
TxD_ECC_TERM[#]
TxD_ECC_RCV[#]

RxD_ECC_PCI[#]
TxD_ECC[#]
RxD_ECC_DDR[#]
RxD_ECC_SDR[#]
TxD_ECC[#]
RxD_ECC_DDR[#]

LSI_SCAN_OUT[2:0]
LSI_SCAN_OUT_LD[2:0]



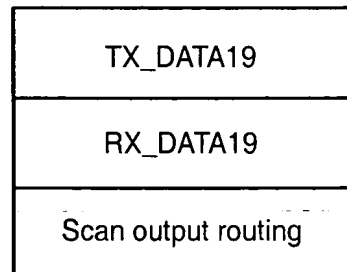
AD_ECC_EN[9]
AD_ECC_OUT[9]
AD_ECC_TERM[9]
AD_ECC_RCV[9]
AD_ECC_IN[9]

CBE_EN[0]
CBE_OUT[0]
CBE_TERM[0]
CBE_RCV[0]
CBE_IN[0]

CBE_EN[1]
CBE_OUT[1]
CBE_TERM[1]
CBE_RCV[1]
CBE_IN[1]

AD_ECC_EN[10]
AD_ECC_OUT[10]
AD_ECC_TERM[10]
AD_ECC_RCV[10]
AD_ECC_IN[10]

•
•
•



AD_ECC_EN[19]
AD_ECC_OUT[19]
AD_ECC_TERM[19]
AD_ECC_RCV[19]
AD_ECC_IN[19]

FIG. 12B